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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,368	07/18/2003	Takashi Tamaki	OKI.550	4056

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,368	TAMAKI, TAKASHI	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 9-13* is/are rejected.

7)☒ Claim(s) *6-8, 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Morris (US 6,064,229).

Regarding claims 1 and 9, Morris discloses, in Fig. 2, a voltage level shifting circuit comprising:

a first power supply node supplied with a first power supply potential level (Vss);

a second power supply node supplied with a second power supply potential level (V_{DD2}) higher than the first power supply potential level (col. 1, lines 28-42);

a third power supply node supplied with a third power supply potential level (V_{DD1}) higher than the second power supply potential level (col. 1, lines 28-42);

a signal input circuit (18) which is coupled between the first power supply node and the second power supply node, which receives a signal having the first and second power supply potential levels, and which outputs a complementary signal (A, A_N) having the first and second power supply potential levels;

a complimentary signal input circuit (N6, N8) which is coupled to the first power supply node and which includes a first pair of MOS transistors, each of the first MOS transistors has a first withstand voltage (col. 1, lines 60+; col. 2, lines 60+) and has a first electrode coupled to the

first power supply node, a second electrode, and a gate electrode receiving the complementary signal;

a load circuit (P2, P3) which is coupled to the third power supply node and which includes a second pair of MOS transistors, each of the second MOS transistors has a second withstand voltage (col. lines 54+; col. 4, lines 20+) higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;

a first voltage down-converting/descending circuit (N5, N7) which is coupled between the load circuit and the complimentary signal input circuit and which prevents a potential level exceeding the first withstand voltage from supplying to the complimentary signal input circuit;

a third MOS transistor (P4) which is coupled between the third power supply node and an output node (26), which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential (24) outputted from the load circuit;

a fourth MOS transistor (N10) which is coupled between the first power supply node and the output node, which has the first withstand voltage, and which electrically connects the first power supply node to the output node **in response to** ("in response to" doesn't mean that fourth MOS transistor is directly connected to one of the voltage potentials of the complimentary signal) one of the voltage potentials of the complimentary signal; and

a second voltage down-converting/descending circuit (N9) which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding the first withstand voltage from supplying to the fourth MOS transistor.

Regarding claims 2, 3, 10, and 11, Morris discloses, in Fig. 2, that the first voltage down-converting/descending circuit comprises a fifth pair of MOS transistors (N5, N7), each of which has a first electrode coupled to the load circuit, a second electrode coupled to the corresponding second electrodes of the first MOS transistors, and a gate electrode supplied with a fixed voltage potential level (V_{DD2}).

Regarding claims 4, 5, 12, and 13, Morris discloses, in Fig. 2, that the second voltage down-converting/descending circuit comprises a sixth MOS transistor (N9) which has a first electrode coupled to the third MOS transistor, a second electrode coupled to the fourth MOS transistor, and a gate electrode supplied with a fixed voltage potential level (V_{DD2}).

Allowable Subject Matter

Claims 6-8 and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 1/31/2005 have been fully considered but they are not persuasive.

The previously cited but not relied upon reference, Morris discloses all the features of the claimed invention including claims 1-5 and 9-13. Therefore the rejection is maintained as discussed above.

Conclusion

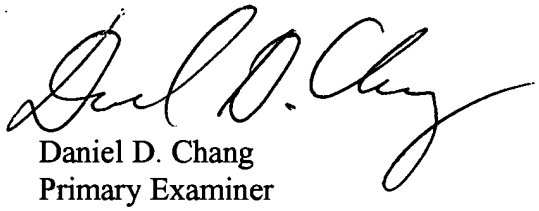
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER